

Fig. 1

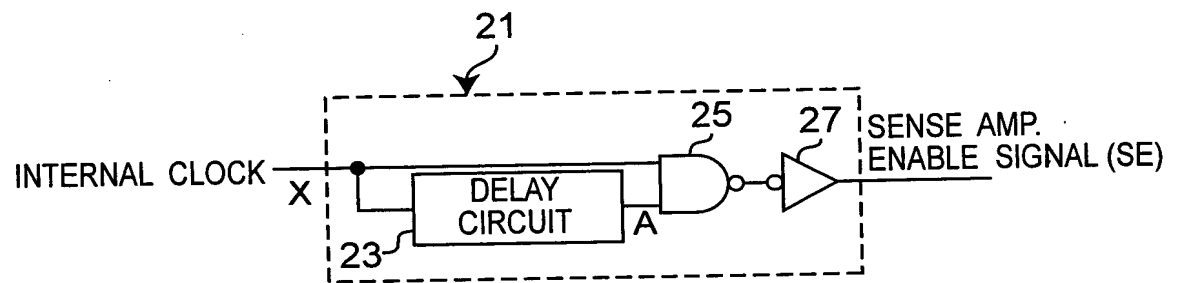


Fig.2

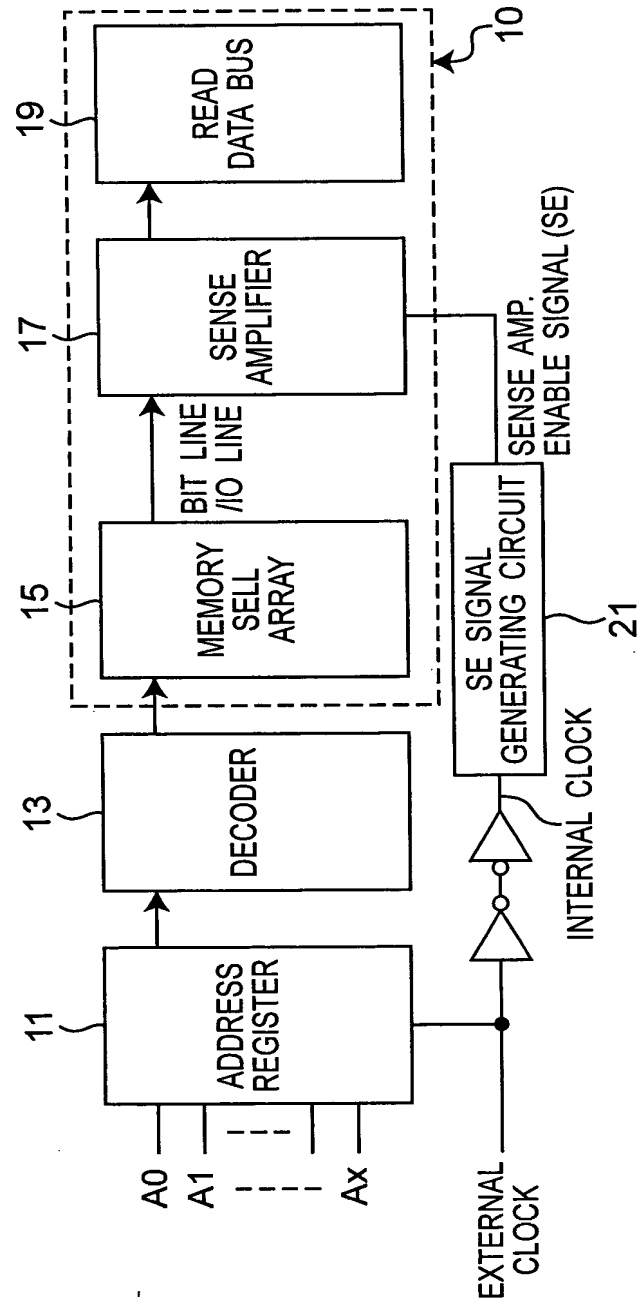


Fig.3

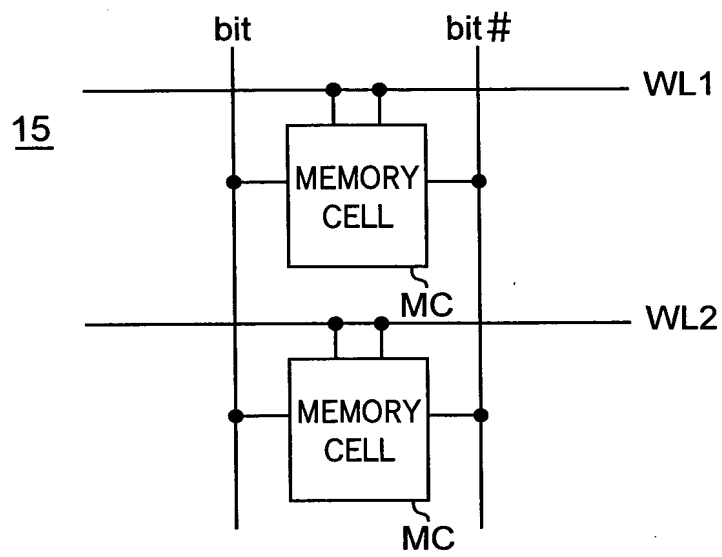


Fig. 4

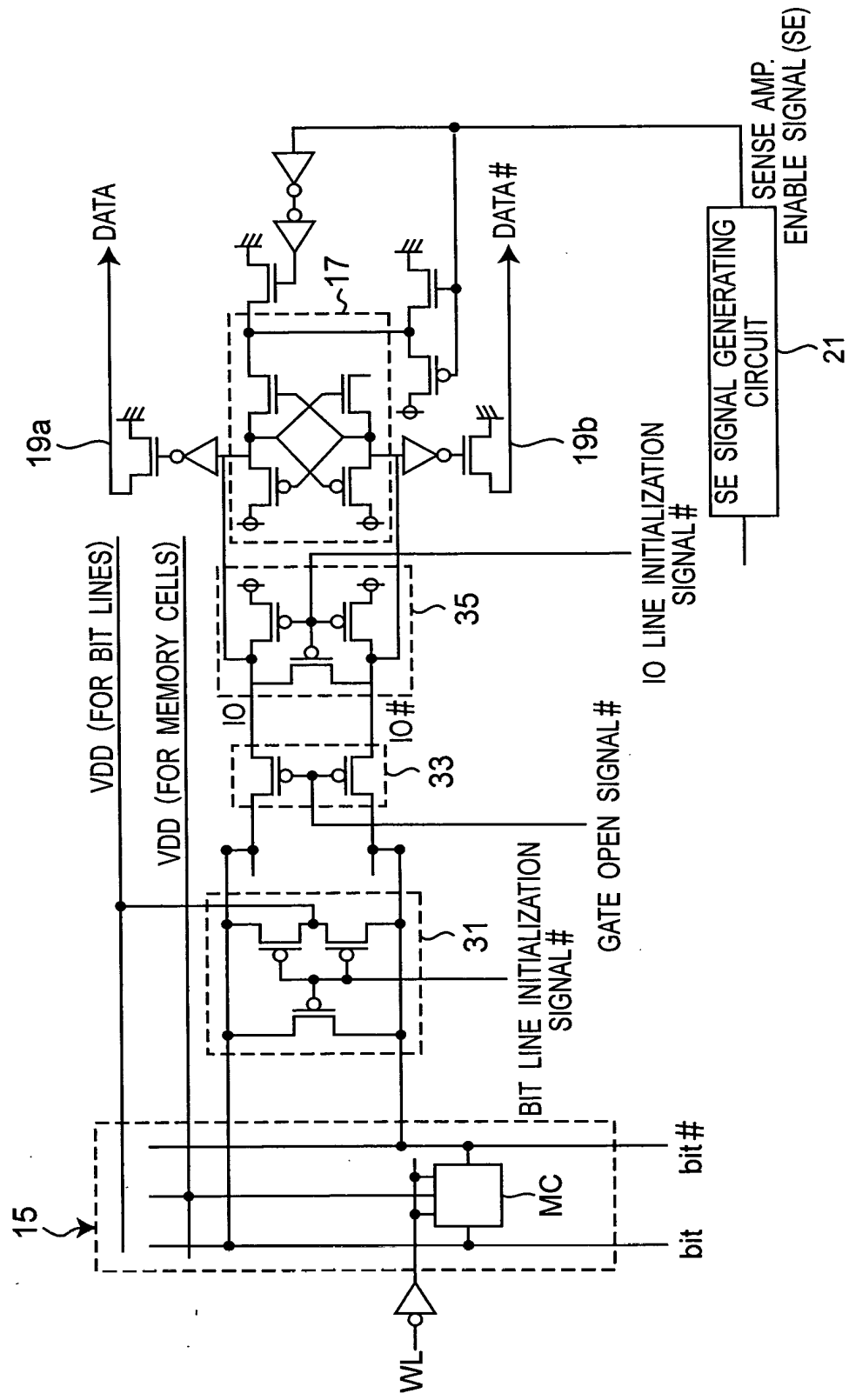


Fig.5A x

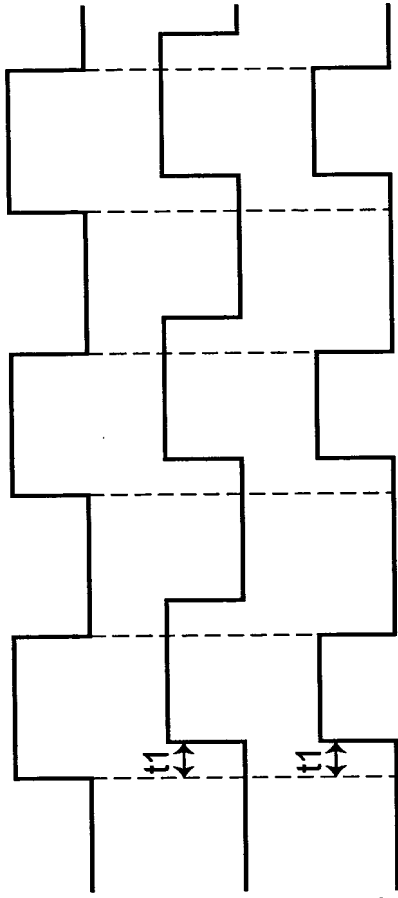


Fig.5B A

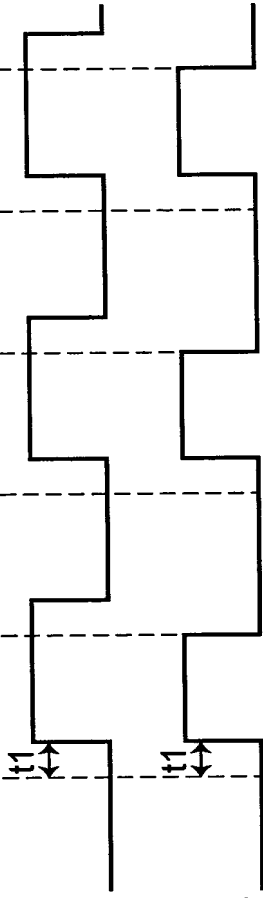


Fig.5C s_E



Fig.6A

WL1

Fig.6B

WL2

Fig.6C

BIT LINES

Fig.6D

BIT LINE
INITIALIZATION
SIGNAL#

Fig.6E

EXTERNAL
CLOCK

Fig.6F

INTERNAL
CLOCK

Fig.6G

INTERNAL
CLOCK (DELAY)

Fig.6H

SENSE AMP.
ENABLE SIGNAL

Fig.6I

IO LINE
INITIALIZATION
SIGNAL#

Fig.6J

IO LINES

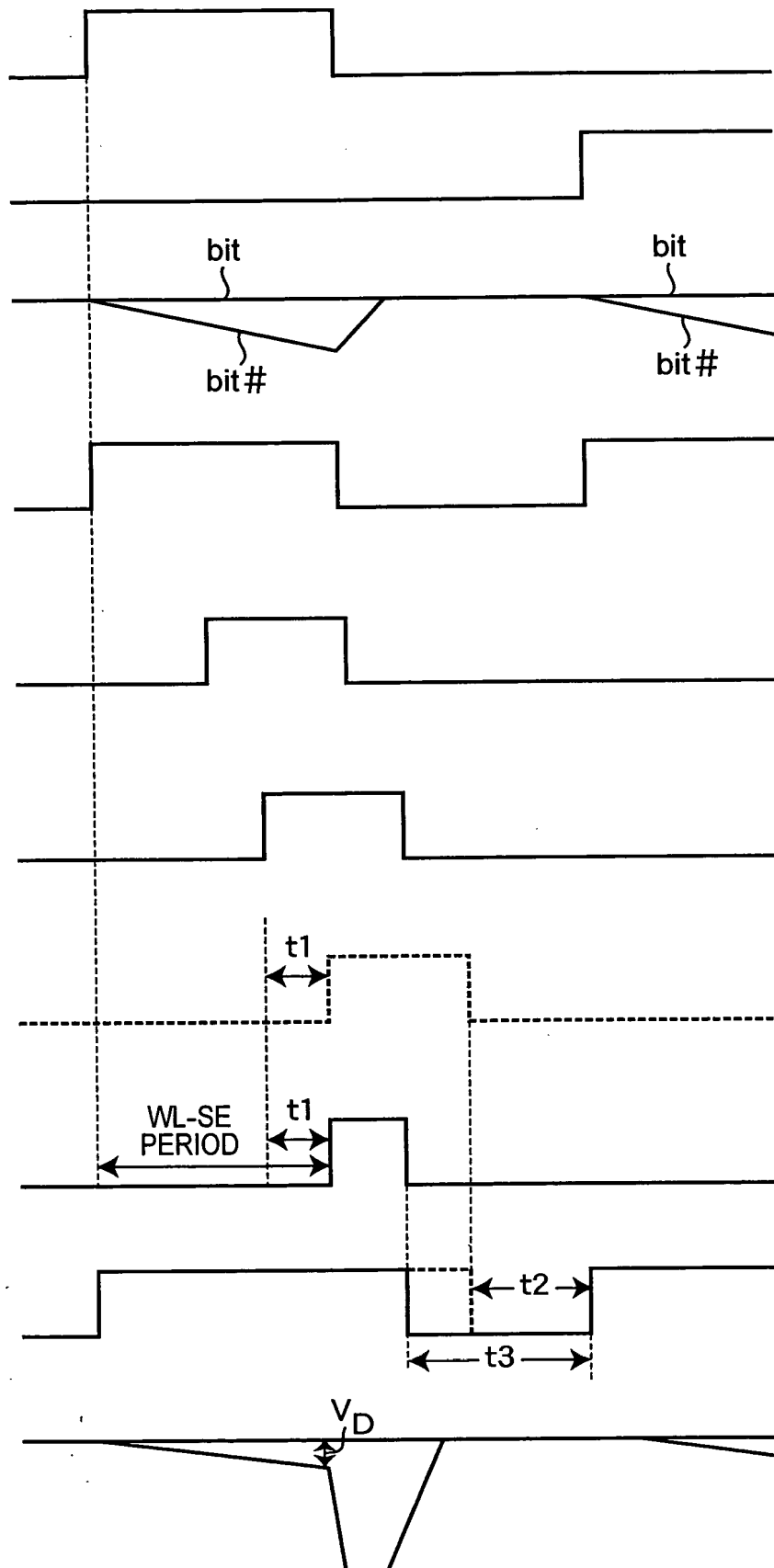


Fig.7

